

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of

Nagamine et al.

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: TEST CIRCUIT FOR LOGICAL INTEGRATED CIRCUIT AND METHOD FOR  
TESTING SAME

Assistant Commissioner of Patents  
Washington, D.C. 20231

JC927 U.S. PTO  
10/026532  
12/27/01

#2

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following document listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. A copy of the listed document is provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of this document is discussed on page 4 of the subject application.

This citation does not constitute an admission that the reference is relevant or material to the claims. It is only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed reference be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,



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Date: 12/27/01

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